CLAIMS

1. A semiconductor memory device comprising:

first and second regions each including a word line extending in a first direction, first and second bit lines extending in a second direction intersecting with said first direction, a memory cell connected to said word line and said first and second bit lines, an amplifier circuit for amplifying information read from said memory cell, first and second IO lines for receiving the read information from said amplifier circuit, and a source line for controlling said amplifier circuit; and

a column select line connected to said first and second regions in common and extending in said second direction,

wherein said amplifier circuit includes first to fourth MOS transistors,

a gate of said first MOS transistor is connected to said first bit line, a gate of said second MOS transistor is connected to said second bit line, and sources of said first and second MOS transistors are connected to said source line,

a drain of said third MOS transistor is connected to said first IO line and a drain of said fourth MOS transistor is connected to said second IO line,

gates of said third and fourth MOS transistors included in the amplifier circuits provided in said first

and second regions are connected to said column select line in common,

a drain of said first MOS transistor is connected to a source of said third MOS transistor,

a drain of said second MOS transistor is connected to a source of said fourth MOS transistor, and

in a first state, potentials of said first and second IO lines included in said first region are higher than a potential of the source line included in said first region, and the first and second IO lines included in said second region and the source line are equal in potential.

2. A semiconductor memory device comprising:

first and second regions each including a word line extending in a first direction, first and second bit lines extending in a second direction intersecting with said first direction, a memory cell connected to said word line and said first and second bit lines, an amplifier circuit for amplifying information read from said memory cell, first and second IO lines for receiving the read information from said amplifier circuit, and a source line for controlling said amplifier circuit; and

a column select line connected to said first and second regions in common and extending in said second direction,

wherein said amplifier circuit includes first to fourth MOS transistors,

a gate of said first MOS transistor is connected to said first bit line, a gate of said second MOS transistor is connected to said second bit line, and sources of said first and second MOS transistors are connected to said source line,

a drain of said third MOS transistor is connected to said first IO line and a drain of said fourth MOS transistor is connected to said second IO line,

gates of said third and fourth MOS transistors included in the amplifier circuits provided in said first and second regions are connected to said column select line in common,

a drain of said first MOS transistor is connected to a source of said third MOS transistor,

a drain of said second MOS transistor is connected to a source of said fourth MOS transistor,

in a first state, potentials of said first and second IO lines included in said first region are higher than a potential of the source line included in said first region, and

potentials of said first and second IO lines included in said second region and a potential of the source line are equal to an absolute value of a value obtained by subtracting a threshold voltage of said first and second MOS transistors from a potential of said first and second bit lines.

3. The semiconductor memory device according to claim 1 or 2,

wherein, in said first state, information is read from the memory cell included in said first region.

4. The semiconductor memory device according to claim 1 or 2,

wherein said first region includes a plurality of said amplifier circuits and a source-line driver for driving said source line,

the plurality of said amplifier circuits included in said first region are connected to said source line in common, and

said source-line driver is disposed in a region surrounded by a sense amplifier column provided with the plurality of said amplifier circuits and a word-driver column provided with a plurality of word drivers for driving said word line.

5. The semiconductor memory device according to any one of claims 1 to 4,

wherein the plurality of said amplifier circuits are connected to said first and second IO lines in common, and

a second amplifier circuit for compensating for offsets of the plurality of said amplifier circuits is connected to said first and second IO lines.

6. The semiconductor memory device according to claim 1 or 2,

wherein said amplifier circuit further includes a fifth MOS transistor, and

a source of said fifth MOS transistor is connected to the drain of said second MOS transistor, a drain of said fifth MOS transistor is connected to the drain of the first MOS transistor, and a gate of said fifth MOS transistor is controlled by a pre-charge signal.

7. The semiconductor memory device according to claim 1 or 2,

wherein said first region further includes a write circuit for writing information to said memory cell, a write column select line for selecting said write circuit, a write control signal line for controlling said write circuit, and a write IO line pair connected to said write circuit,

said write circuit further includes sixth to ninth MOS transistors,

gates of said sixth and seventh MOS transistors are connected to said write column select line, a drain of said sixth MOS transistor is connected to one of said write IO line pair, and a drain of said seventh MOS transistor is connected to the other of said write IO line pair,

gates of said eighth and ninth MOS transistors are connected to said write control signal line, a source of

said eighth MOS transistor is connected to said first bit line, and a source of said ninth MOS transistor is connected to said second bit line, and

a source of said sixth MOS transistor is connected to a drain of said eighth MOS transistor, and a source of said seventh MOS transistor is connected to a drain of the ninth MOS transistor.

8. The semiconductor memory device according to claim 7,

wherein said write column select line is connected to said column select line.

9. The semiconductor memory device according to claim 7 or 8,

wherein said write circuit further includes a tenth MOS transistor, and

a source of said tenth MOS transistor is connected to the source of said sixth MOS transistor, a drain of said tenth MOS transistor is connected to the source of said seventh MOS transistor, and a gate of said tenth MOS transistor is controlled by a pre-charge signal.

10. A semiconductor memory device comprising:

first and second regions each including a word line extending in a first direction, a plurality of bit line pairs extending in a second direction intersecting with said first direction, a plurality of memory cells connected

to said word line and said plurality of bit line pairs, an amplifier circuit for amplifying information read from said memory cells, first and second IO lines for receiving the read information from said amplifier circuit, a source line for controlling said amplifier circuit, and selecting means for selecting a signal inputted to said amplifier circuit; and

a column select line connected to first and second regions in common and extending in said second direction,

wherein said amplifier circuit includes first to fourth MOS transistors,

gates of said first and second MOS transistors receives an input of said selecting means, and sources of said first and second MOS transistors are connected to said source line,

a drain of said third MOS transistor is connected to said first IO line, and a drain of said fourth MOS transistor is connected to said second IO line,

each gate of said third and fourth MOS transistors included in said amplifier circuit is connected to said column select line in common,

a drain of said first MOS transistor is connected to a source of said third MOS transistor,

a drain of said second MOS transistor is connected to a source of said fourth MOS transistor, and

signals of said plurality of bit line pairs are inputted to said selecting means.

11. The semiconductor memory device according to claim 10,

wherein said semiconductor memory device is such that, in a first state, potentials of said first and second IO lines included in said first region are higher than a potential of said source line included in said first region, and

potentials of said first and second IO lines included in said second region and of said source line are equal to or more than an absolute value of a value obtained by subtracting a threshold voltage of said third and fourth MOS transistors from a potential of said plurality of bit line pairs included in said second region.

12. The semiconductor memory device according to claim 10 or 11,

wherein said memory cell includes two transistors and two capacitors, and

said selecting means is a multiplexer.

13. A semiconductor memory device comprising:

first and second regions each including a word line extending in a first direction, a plurality of bit lines extending in a second direction intersecting with said first direction and having first and second bit lines, a plurality of memory cells connected to said word line and said plurality of bit lines, first and second circuit

columns each provided with an amplifier circuit for amplifying information read from said memory cells and a write circuit for writing the information to said memory cells, first and second IO line pairs connected to said circuit columns and extending in said first direction, and a source line connected to said amplifier circuits; and

first and second read column select lines and first and second write column select lines connected to said first and second regions in common,

wherein said first and second read column select lines and said first and second write column select lines extend in said second direction,

each of the amplifier circuits provided in the first and second circuit columns has first to fourth MOS transistors,

a gate of said first MOS transistor is connected to said first bit line, a gate of said second MOS transistor is connected to said second bit line, and sources of said first and second MOS transistors are connected to said source line,

a drain of said first MOS transistor is connected to a source of said third MOS transistor,

a drain of said second MOS transistor is connected to a source of said fourth MOS transistor,

a drain of the third MOS transistor of the amplifier circuit included in said first circuit column is connected to one of the first IO line pair connected to said write

column select line included in said second circuit column, and a drain of said fourth MOS transistor is connected to the other of the first IO line pair connected to the write circuit included in said second circuit column,

a drain of the third MOS transistor of the amplifier circuit included in said second circuit column is connected to one of the second IO line pair connected to the write circuit included in said first circuit column, and the drain of the fourth MOS transistor is connected to the other of the second IO line pair connected to the write circuit included in said first circuit column,

the write circuit included in said first circuit column is connected to said first write column select line,

the write circuit included in said second circuit column is connected to said second write column select line,

gates of the third and fourth MOS transistors in the amplifier circuit of said first circuit column included in said first region and gates of the third and fourth MOS transistors in the amplifier circuit of said first circuit column included in said second region are connected to said first read column select line in common,

gates of the third and fourth MOS transistors in the amplifier circuit of said second circuit column included in said first region and gates of the third and fourth MOS transistors in the amplifier circuit of said second circuit column included in said second region are connected to said second read column select line in common,

in a first state, said first and second read column select lines are activated, and potentials of said first and second IO line pairs included in said first region are higher than a potential of the source line included in said first region, and

the first and second IO line pairs included in said second region and the source line are equal in potential, or potentials of the first and second IO lines included in said second region and a potential of said source line is equal to an absolute value of a value obtained by subtracting a threshold voltage of said first and second MOS transistors from a potential of said first and second bit lines.

14. A semiconductor memory device comprising:

a first amplifier circuit having first and second N-channel MOS transistors and first and second P-channel MOS transistors; and

a second amplifier circuit for amplifying, to a power-supply voltage amplitude, information read from a memory cell,

wherein a gate of said first N-channel MOS transistor and a gate of said second N-channel MOS transistor are connected to a first power-supply potential, a source of said first N-channel MOS transistor is connected to a first input terminal, and a source of said second N-channel MOS transistor is connected to a second input terminal,

a gate of said first P-channel MOS transistor and a gate of said second P-channel MOS transistor are connected to a ground potential, a source of said first P-channel MOS transistor and a source of said second P-channel MOS transistor are connected to said first power-supply potential,

a drain of said first N-channel MOS transistor is connected to a drain of said first P-channel MOS transistor, and a drain of said second N-channel MOS transistor is connected to a drain of said second N-channel MOS transistor, and

said first and second N-channel MOS transistors receive inputs of the information read from said memory cell prior to said first and second P-channel MOS transistors.

15. The semiconductor memory device according to claim 14,

wherein said semiconductor memory device further comprises a first circuit including third to sixth N-channel MOS transistors,

a gate of said third N-channel MOS transistor is connected to the drain of said first P-channel MOS transistor, a gate of said fourth N-channel MOS transistor is connected to the drain of the second P-channel MOS transistor,

a source of said third N-channel MOS transistor and a source of said fourth N-channel MOS transistor are

connected to said second amplifier circuit,

a drain of said third N-channel MOS transistor and a drain of said fourth N-channel MOS transistor are connected to said first power-supply potential,

a gate of said fifth N-channel MOS transistor and a gate of said sixth N-channel MOS transistor are connected to a second power-supply potential,

said fifth MOS transistor and a drain of said sixth MOS transistor are connected to said second amplifier circuit, and

a source of said fifth MOS transistor and a source of said sixth MOS transistor are connected to said ground potential.